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Washington D.C., 20231

Case Docket No.: 81674-027 1623
Date: September 18, 2000
Express Mail Label No.: EL 594 170 115 US

Dear Sir:

Transmitted herewith for filing is the patent application of
Inventor(s): John Halbert of Beaverton, Oregon and Randy M. Bonella of Portland, Oregon
For: MEMORY MODULE AND MEMORY COMPONENT BUILT-IN SELF TEST

Enclosed are:

X 2 Sheets of formal drawings
X An assignment of the invention to Intel Corporation. X Will follow.
X An unsigned Declaration and Power of Attorney.

CALCULATION OF FEES

	ITEM	NO. OF CLAIMS FILED MINUS BASE*	NO. OF CLAIMS OVER BASE	X SM/LG ENTITY FEE	$ AMOUNT	FEE
A	TOTAL CLAIMS FEE	53 -20*=	33	x $9 or x $18	$594	
B	INDEPENDENT CLAIMS FEE**	7 - 3*=	4	x$39 or x 78	$312	
C	SUBTOTAL – ADDITIONAL CLAIMS FEE (ADD FINAL COLUMN IN LINES A + B)					$906
D	MULTIPLE-DEPENDENT CLAIMS FEE			SMALL ENTITY FEE = $130 LARGE ENTITY FEE = $260		$0
E	BASIC FEE*			SMALL ENTITY FEE = $345 LARGE ENTITY FEE = $690		$690
F	TOTAL FILING FEE (ADD TOTALS FOR LINES C, D, AND E)					$1596
G	ASSIGNMENT RECORDING FEE				$40	$0
	**LIST INDEPENDENT CLAIMS (1, 9, 16, 24, 31, 39 and 48)					

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__ The issue fee set in 37 CFR 1.18 at or before mailing of the Notice of Allowance, pursuant to 37 CFR 1.311(b).

__ Any filing fees under 37 CFR 1.16 for presentation of extra claims.

Respectfully submitted,

Dated: September 18, 2000

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PATENT
81674-027 1623

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: John HALBERT and Randy M. BONELLA	Group No.: NOT ASSIGNED
Serial No.: NOT ASSIGNED	Examiner: NOT ASSIGNED
Filed: September 18, 2000	
For: MEMORY MODULE AND MEMORY COMPONENT BUILT-IN SELF TEST	

CERTIFICATE OF MAILING VIA U.S. EXPRESS MAIL
"Express Mail" Mailing Label No. EL 594 170 115 US
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I hereby certify that

X Letter of transmittal
X Patent application (17 pages of specification; 53 claims; 1 pages of abstract)
X 2 sheets of formal drawings
X An unsigned Declaration/Power of Attorney
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September 18, 2000
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APPLICATION FOR
UNITED STATES PATENT
IN THE NAME OF

JOHN HALBERT AND RANDY M. BONELLA

FOR

MEMORY MODULE AND MEMORY COMPONENT BUILT-IN SELF TEST

Prepared By:

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Client Reference No.: P-9613/15

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TITLE OF THE INVENTION

MEMORY MODULE AND MEMORY COMPONENT BUILT-IN SELF TEST

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to memory systems, and more specifically, to memory modules and memory components, such as a memory device or a memory buffer, having built-in self test functionality.

2. Discussion of the Related Art

Integrated circuit devices such as random access memories (RAMs) usually undergo device verification testing during manufacture. Typically, such verification tests are designed to detect both static and dynamic defects in a memory array. Static defects include, for example, open circuit and short circuit defects in the integrated circuit device. Dynamic defects include defects such as weak pull-up or pull-down transistors that create timing sensitive defects.

A specialized integrated circuit device tester is normally employed to perform manufacturing verification tests. For example, such an integrated circuit device tester may be used to perform read/write verification cycle tests on the memory array. Relatively low-speed (e.g., 20 MHz), low-cost integrated circuit device testers are usually sufficient for detecting static defects in the memory array. However, extremely expensive integrated device testers are needed to detect dynamic defects in very high-speed memory arrays. Such expensive high-speed integrated circuit testers increase the overall manufacturing costs for such devices. In addition,

for integrated circuit devices that include large memory arrays, the cycle time required to perform such read/write tests increases in proportion to the size of the array.

Attempts to overcome some of the difficulties associated with testing integrated circuit devices have included implementing built-in self-test (BIST) circuitry. For example, an integrated circuit cache memory array may contain circuitry to perform a standard static random access memory (SRAM) 13N March test algorithm on the memory array. A state machine is typically used to generate the 13N March test algorithm along with circuitry to sample data output and to generate a signature of the results. The signature is then compared against an expected value to determine whether defects exist in the memory array. Such BIST circuitry usually enables high-speed testing while obviating expensive high-speed testers.

Unfortunately, these BIST routines have generally only been able to apply a preprogrammed test sequence on the memory array. As the process of manufacturing such a memory array evolves, manufacturing test engineers typically develop improved strategies for detecting both static and dynamic defects in the memory array.

Moreover, such improved strategies for detecting defects can only be applied to testing that occurs while the device is placed in an expensive integrated circuit device tester. Therefore, engineers have been unable to achieve the benefits of improved test strategies without the use of an expensive tester, or without redesigning the integrated circuit device. Because of the advances in memory technology, and particularly in the area of narrow high-speed buses, which typically run at speeds of about 1.6 GHz, for use with dynamic random access memory devices (DRAMs), it is very expensive to obtain a high-speed tester capable of testing a memory module or a memory component at such high operating frequencies. Therefore, the added use of expensive high-speed hardware testers increases the time required to ascertain hardware failures,

not to mention greatly increasing the overall manufacturing cost of these memory modules and memory components.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 illustrates a memory module having built-in self test according to an embodiment of the present invention; and

Fig. 2 illustrates a memory component having built-in self test according to an embodiment of the present invention.

DETAILED DESCRIPTION

Fig. 1 illustrates a memory module having built-in self test (BIST) according to an embodiment of the present invention. By utilizing the memory module 100 of Fig. 1, an expensive external high-speed tester is not required to test the memory module 100. The memory module 100 is configured so as to utilize BIST without any external equipment.

The memory module 100 shown in Fig. 1 utilizes a set of buffers 130, 140, 150 in order to provide an interface with a processor component, such as a memory controller (not shown), which may be operating at a different voltage and/or frequency than the memory devices 110, 120, such as dynamic random access memory (DRAM) devices. In the embodiment of Fig. 1, a three-buffer configuration is utilized for the memory module 100: two data buffers 1st 130, 2nd 140, and an address and command buffer 150. However, the 1st and 2nd data buffers 130, 140 and the address and command buffer 150 may be incorporated into a single buffer device, or additional buffer components may be utilized as well.

In one embodiment, the built-in self test (BIST) logic and circuitry are incorporated with the address and command buffer 150. The address and command buffer preferably includes an address and command generator 154 to generate the address and commands and the test data to be transmitted to the memory devices 110, 120 for testing. However, instead of generating the test data, the BIST logic may utilize existing data extracted from the memory controller off of the data bus as the test data as well. Along with generating the test data, the address and command generator 154 also generates compare test data, which is used to compare the test data read from the memory devices 110, 120, with the test data (which is identical to the compare test data) initially transmitted from the address/command generator 154 to the memory devices 110,120 for storage.

In one embodiment, the test data generated by the address/command generator 154 is transmitted to the memory devices 110, 120 for storage therein. Then, the test data stored (written) in the memory devices 110, 120 are read from the memory devices 110, 120 and compared with the compare test data, which is identical to the test data, also generated by the address/command generator 154. A comparator 145, such as an "exclusive OR" (XOR) comparator, may be provided in each one of the data buffers 130,140 to compare the test data read from the memory devices 110, 120 with the compare test data provided by the address/command generator 154. A determination of whether the comparison is a match or a failure is made by the comparator 145, and a result then is preferably transmitted to a test result/status register 156, that may be provided within the address and command buffer 150. The test result/status register 156 may then provide a test status or result signal to an external device, such as a memory controller. The test status/result signal generated by the test result/status register 156 may utilize a two-bit packet, indicating, for example, the following states: BIST not

enabled (00); BIST executing (01); BIST failed (10); and BIST passed (11). Although Fig. 1 illustrates a memory module 100 having two memory devices 110, 120, the memory module 100 is not limited to only two memory devices, and any suitable number may be used.

Additionally, rather than using a high-speed clock signal to perform testing, the memory module 100 may use a slow speed clock signal, generating just one clock, and using a clock multiplier 152 within the address and command buffer 150 to multiply and distribute the clock signal to the memory devices 110, 120. Accordingly, by utilizing the memory module 100 illustrated in Fig. 1, the memory module 100 may be tested independently of other systems, and expensive high-speed testers are not required to test the memory devices 110,120 and their connections within the memory module 100 itself.

Fig. 2 illustrates a memory component having BIST according to an embodiment of the present invention. As illustrated in Fig. 2, BIST logic may be provided completely within a single memory component, such as a buffer 210 and a memory device 220. That is, each memory component may be taken independently of any other component and tested on its own. The buffer 210 may be an address and command buffer 150, or a data buffer 130, 140, as discussed above with respect to Fig. 1.

The BIST logic includes a controller 260 to perform the BIST operations. The controller 260 preferably receives a clock signal, and also provides test result signals from the memory component, such as a buffer 210 or a memory device 220. The controller 260, like the address and command generator 154 of Fig. 1, is adapted to generate test data and compare test data to test the functional logic or memory array 250 (depending on the type of memory component, e.g., a buffer or memory device) of the buffer component 210, or memory device 220. The test data is preferably provided to the functional logic or memory array 250, which is then

transmitted to an input/output interface 230, 240. The test data may also be transmitted directly to the input/output interface 230, 240 from the controller 260 to test the input/output interface 230, 240.

The input/output interface 230, 240 is configured with a loopback so that the test data may be directed back from an input/output connection to a compare register 270 to compare the test data from the input/output interface 230, 240, and ultimately, the functional logic or memory array 250. The controller 260 is adapted to generate and provide compare test data to the compare register 270 so that the compare register 270 may compare the test data received from the input/output interface 230, 240 with the compare test data to determine whether there was a match, and whether the test was successful. Accordingly, the compare register 270 makes a determination regarding the results of the test, and the test results are reported, preferably by the controller 260. The compare register 270 and the controller 260 may be embodied within a single device or a common circuit.

Therefore, by having memory components such as a buffer 210 and a memory device 220 with BIST, localized self-testing may be performed after the buffer 210 and the memory device 220 is manufactured. However, component-level built-in self test may be performed at various stages of manufacture and packaging, including at the wafer probe stage, during post-packaging, and even during post-assembly. Accordingly, the memory components 210, 220 of Fig. 2 may be tested independently of other components, and expensive high-speed testers are not required to test the memory components 210, 220.

While the description above refers to particular embodiments of the present invention, it will be understood that many modifications may be made without departing from the spirit thereof. The accompanying claims are intended to cover such modifications as would fall within

the true scope and spirit of the present invention. The presently disclosed embodiments are therefore to be considered in all respects as illustrative and not restrictive, the scope of the invention being indicated by the appended claims, rather than the foregoing description, and all changes that come within the meaning and range of equivalency of the claims are therefore intended to be embraced therein.

WHAT IS CLAIMED IS:

1. A memory component with built-in self test, comprising:

an input/output interface coupled to the memory array and having a loopback;

a controller to transmit input/output test data to the input/output interface, and to receive the input/output test data from the loopback of the input/output interface; and

a compare register to compare the input/output test data transmitted to the input/output interface with the input/output test data received from the input/output interface.

2. The memory component according to claim 1, wherein the memory component is a dynamic random access memory (DRAM).

3. The memory component according to claim 1, wherein the memory component is a buffer.

4. The memory component according to claim 3, wherein the buffer is an address and command buffer.

5. The memory component according to claim 3, wherein the buffer is a data buffer.

6. The memory component according to claim 3, wherein the buffer is an address and command and data buffer.

7. The memory component according to claim 1, wherein the compare register generates a test result based on the input/output test data transmitted to the input/output interface compared with the input/output test data received from the input/output interface.

8. The memory component according to claim 1, wherein the controller is adapted to transmit memory array test data to a memory array to store the test data therein, and to read the memory array test data from the memory array, and the compare register is adapted to compare the memory array test data transmitted to the memory array with the memory array test data read from the memory array.

9. A memory component with built-in self test, comprising:

a memory array;

an input/output interface coupled to the memory array and having a loopback;

a controller to transmit memory array test data to the memory array to store the memory array test data, and to read the memory array test data from the memory array; and

a compare register to compare the memory array test data transmitted to the memory array with the memory array test data read from the memory array.

10. The memory component according to claim 9, wherein the memory component is a dynamic random access memory (DRAM).

11. The memory component according to claim 9, wherein the memory component is a buffer.

12. The memory component according to claim 11, wherein the buffer is an address and command buffer.

13. The memory component according to claim 11, wherein the buffer is a data buffer.

14. The memory component according to claim 11, wherein the buffer is an address and command and data buffer.

15. The memory component according to claim 9, wherein the compare register generates a test result based on the memory array test data transmitted to the memory array compared with the memory array test data read from the memory array.

16. A method of testing a memory component with built-in self test, comprising:

transmitting input/output test data to an input/output interface having a loopback;

receiving the input/output test data from the loopback of the input/output interface; and

comparing the input/output test data transmitted to the input/output interface with the input/output test data received from the input/output interface.

17. The method according to claim 16, wherein the memory component is a dynamic random access memory (DRAM).

18. The method according to claim 16, wherein the memory component is a buffer.

19. The method according to claim 18, wherein the buffer is an address and command buffer.

20. The method according to claim 18, wherein the buffer is a data buffer.

21. The method according to claim 18, wherein the buffer is an address and command and data buffer.

22. The method according to claim 16, wherein the compare register generates a test result based on the input/output test data transmitted to the input/output interface compared with the input/output test data received from the input/output interface.

23. The method according to claim 16, further including:

transmitting memory array test data to a memory array;

storing the memory array test data in the memory array;

reading the memory array test data from the memory array; and

comparing the memory array test data transmitted to the memory array with the memory array test data read from the memory array.

24. A method of testing a memory component with built-in self test, comprising:

transmitting memory array test data to a memory array;

storing the memory array test data in the memory array

reading the memory array test data from the memory array; and

comparing the memory array test data transmitted to the memory array with the memory array test data read from the memory array.

25. The method according to claim 24, wherein the memory component is a dynamic random access memory (DRAM).

26. The method according to claim 24, wherein the memory component is a buffer.

27. The method according to claim 26, wherein the buffer is an address and command buffer.

28. The method according to claim 26, wherein the buffer is a data buffer.

29. The method according to claim 26, wherein the buffer is an address and command and data buffer.

30. The method according to claim 24, wherein the compare register generates a test result based on the memory array test data transmitted to the memory array compared with the memory array test data read from the memory array.

31. A memory module with built-in self test, comprising:

at least one memory component;

an address and command buffer adapted to transmit address and command data and test data to the at least one memory component, wherein the address and command buffer includes a register to receive a test result; and

at least one data buffer to receive the test data from the address and command buffer, to receive the test data from the at least one memory component, and to compare the test data received from the address and command buffer with the test data received from the at least one memory component to generate the test result.

32. The memory module according to claim 31, wherein the address and command buffer and the data buffer are within a single buffer chip.

33. The memory module according to claim 31, wherein the at least one memory component is a dynamic random access memory (DRAM).

34. The memory module according to claim 31, wherein the address and command buffer includes a clock multiplier to receive a clock signal and to multiply the clock signal for transmission to the at least one memory component and the at least one data buffer.

35. The memory module according to claim 31, wherein the address and command buffer includes an address and command generator to generate the address and command data.

36. The memory module according to claim 31, wherein the test data is obtained from a data bus through a memory controller.

37. The memory module according to claim 31, wherein the register receives the test result from the at least one data buffer and reports the test result as one of the following conditions: built-in self test not enabled, built-in self test enabled, built-in self test failed, and built-in self test passed.

38. The memory module according to claim 31, wherein the at least one data buffer utilizes an exclusive-OR (XOR) comparator to compare the test data received from the address and command buffer with the test data received from the at least one memory component.

39. A method of testing a memory module with built-in self test, the method comprising:

transmitting address and command data and test data to a memory component from an address and command buffer;

receiving the test data from the address and command buffer;

receiving the test data from the memory component; and

comparing the test data received from the address and command buffer with the test data received from the memory component to generate a test result.

40. The method according to claim 39, wherein receiving the test data from the address and command buffer, receiving the test data from the memory component, and comparing the test data are performed in a data buffer.

41. The method according to claim 40, wherein the data buffer and the address and command buffer are within a single buffer chip.

42. The method according to claim 39, wherein the memory component is a dynamic random access memory (DRAM).

43. The method according to claim 39, further including:

receiving a clock signal by a clock multiplier of the address and command buffer;

multiplying the clock signal; and

transmitting the clock signal to the memory component and a data buffer.

44. The method according to claim 39, further including:

generating the address and command data from an address and command data generator of the address and command buffer.

45. The method according to claim 39, further including:

obtaining the test data from a data bus through a memory controller.

46. The method according to claim 39, further including:

receiving the test result in a register of the address and command buffer; and

reporting the test result from the register as one of the following conditions: built-in self test not enabled, built-in self test enabled, built-in self test failed, and built-in self test passed.

47. The method according to claim 39, wherein comparing the test data received from the address and command buffer with the test data received from the memory component is performed by a data buffer utilizing an exclusive-OR (XOR) comparator.

48. A memory module with built-in self test, comprising:

at least one memory component;

an address and command buffer adapted to transmit address and command data and test data to the at least one memory component, wherein the address and command buffer includes,

a register to receive a test result,

a clock multiplier to receive a clock signal and to multiply the clock signal for transmission, and

an address and command generator to generate the address and command data; and

at least one data buffer to receive the test data from the address and command buffer, to receive the test data from the at least one memory component, and to compare the test data received from the address and command buffer with the test data received from the at least one memory component to generate the test result.

49. The memory module according to claim 48, wherein the address and command buffer and the data buffer are within a single buffer chip.

50. The memory module according to claim 48, wherein the at least one memory component is a dynamic random access memory (DRAM).

51. The memory module according to claim 48, wherein the test data is obtained from a data bus through a memory controller.

52. The memory module according to claim 48, wherein the register receives the test result from the at least one data buffer and reports the test result as one of the following conditions: built-in self test not enabled, built-in self test enabled, built-in self test failed, and built-in self test passed.

53. The memory module according to claim 48, wherein the at least one data buffer utilizes an exclusive-OR (XOR) comparator to compare the test data received from the address and command buffer with the test data received from the at least one memory component.

ABSTRACT OF THE INVENTION

A memory component with built-in self test includes a memory array. An input/output interface is coupled to the memory array and has a loopback. A controller is provided to transmit memory array test data to the memory array to store the memory array test data, and to read the memory array test data from the memory array. A compare register is also provided to compare the memory array test data transmitted to the memory array with the memory array test data read from the memory array.

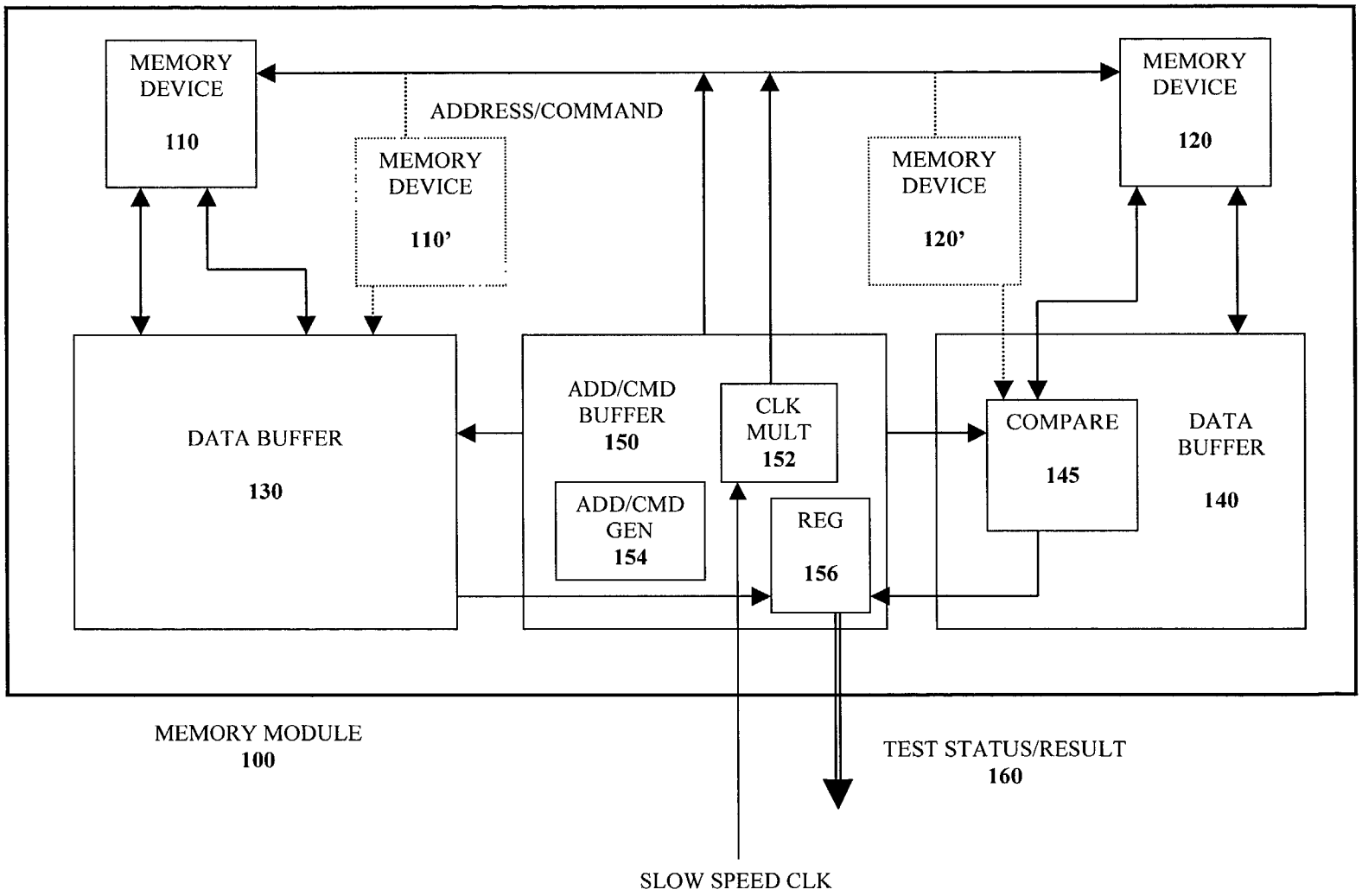
MEMORY DEVICE 110
ADDRESS/COMMAND
MEMORY DEVICE 110'
MEMORY DEVICE 120
MEMORY DEVICE 120'
DATA BUFFER 130
ADD/CMD BUFFER 150
CLK MULT 152
ADD/CMD GEN 154
REG 156
COMPARE 145
DATA BUFFER 140
MEMORY MODULE 100
TEST STATUS/RESULT 160
SLOW SPEED CLK

FIG. 1

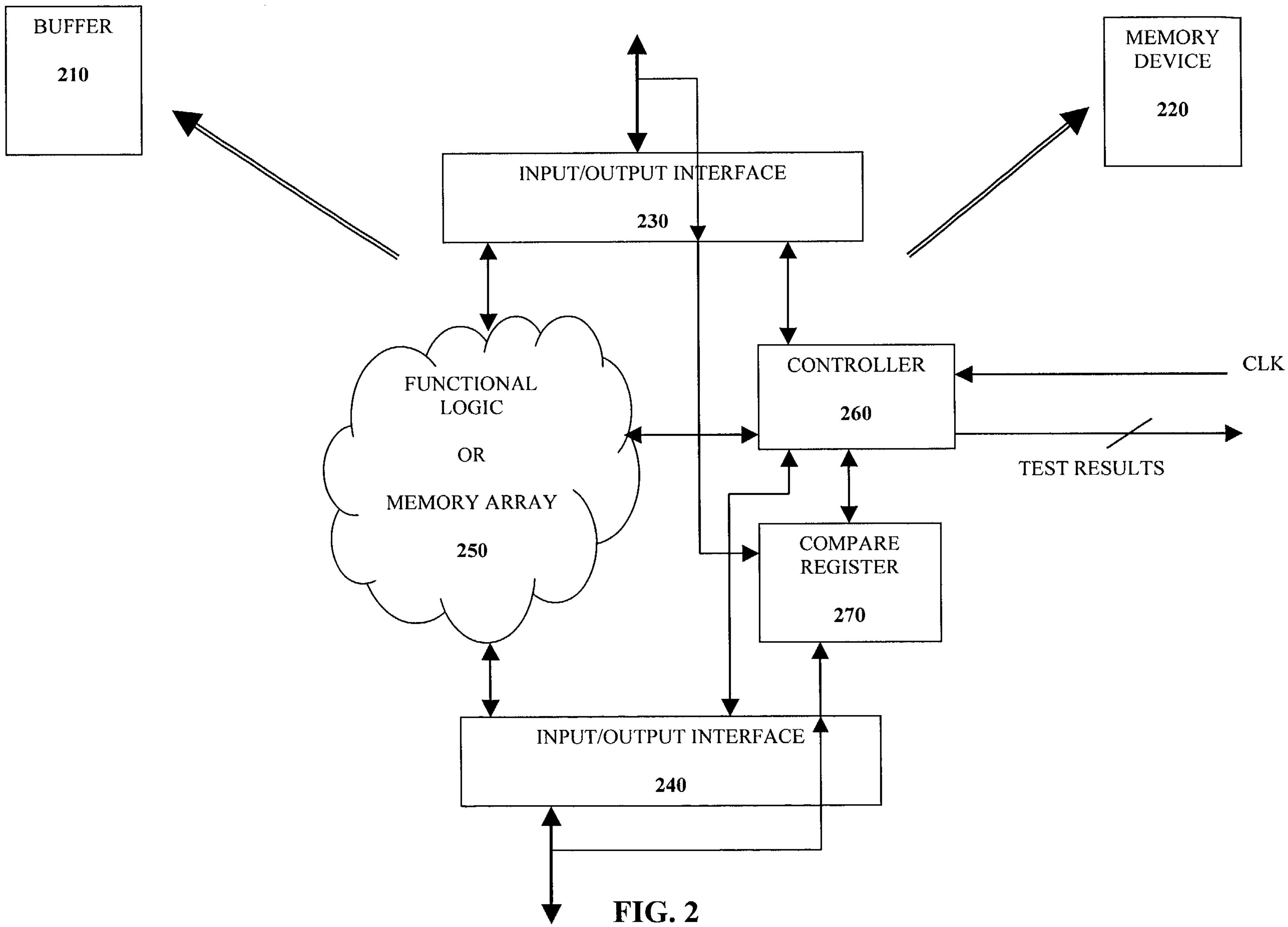
BUFFER
210
MEMORY DEVICE
220
INPUT/OUTPUT INTERFACE
230
FUNCTIONAL LOGIC
OR
MEMORY ARRAY
250
CONTROLLER
260
CLK
TEST RESULTS
COMPARE REGISTER
270
INPUT/OUTPUT INTERFACE
240

FIG. 2

FOR UTILITY/DESIGN
CIP/PCT NATIONAL/PLANT
ORIGINAL/SUBSTITUTE/SUPPLEMENTAL
DECLARATIONS

RULE 63 (37 C.F.R. 1.63) DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PM & S FORM

As a below named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name, and I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the **INVENTION ENTITLED** MEMORY MODULE AND MEMORY COMPONENT BUILT-IN SELF TEXT

the specification of which (CHECK applicable BOX(ES))

X A. ☒ is attached hereto.

BOX(ES) → B. ☐ was filed on _____ as U.S. Application No. ___/_____

→ → C. ☐ was filed as PCT International Application No. PCT/ ___/_____ on _____

and (if applicable to U.S. or PCT application) was amended on _____

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose all information known to me to be material to patentability as defined in 37 C.F R. 1 56 Except as noted below, I hereby claim foreign priority benefits under 35 U S.C 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International Application which designated at least one other country than the United States, listed below and have also identified below any foreign application for patent or inventor's certificate, or PCT International Application, filed by me or my assignee disclosing the subject matter claimed in this application and having a filing date (1) before that of the application on which priority is claimed, or (2) if no priority claimed, before the filing date of this application:

PRIOR FOREIGN APPLICATION(S) Number	Country	Day/MONTH/Year Filed	Date first Laid-open or Published	Date Patented or Granted	Priority NOT Claimed

If more prior foreign applications, X box *at bottom* and continue on attached page.

Except as noted below, I hereby claim domestic priority benefit under 35 U S C. 119(e) or 120 and/or 365(c) of the indicated United States applications listed below and PCT international applications listed above or below and, if this is a continuation-in-part (CIP) application, insofar as the subject matter disclosed and claimed in this application is in addition to that disclosed in such prior applications, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in 37 C F R 1 56 which became available between the filing date of each such prior application and the national or PCT international filing date of this application:

PRIOR U.S. PROVISIONAL, NONPROVISIONAL AND/OR PCT APPLICATION(S) Application No. (series code/serial no.)	Day/MONTH/Year Filed	Status pending, abandoned, patented	Priority NOT Claimed

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

And I hereby appoint Pillsbury Madison & Sutro LLP, Intellectual Property Group, 1100 New York Avenue, N W , Ninth Floor, East Tower, Washington, D.C 20005-3918, telephone number (202) 861-3000 (to whom all communications are to be directed), and the below-named persons (of the same address) individually and collectively my attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith and with the resulting patent, and I hereby authorize them to delete names/numbers below of persons no longer with their firm and to act and rely on instructions from and communicate directly with the person/assignee/attorney/firm/ organization who/which first sends/sent this case to them and by whom/which I hereby declare that I have consented after full disclosure to be represented unless/until I instruct the above Firm and/or a below attorney in writing to the contrary.

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G. Lloyd Knight	17698	Kendrew H. Colton	30368	Richard H. Zaitlen	27248	Paul L. Sharer	36004
Kevin E. Joyce	20508	G. Paul Edgell	24238	Roger R. Wise	31204	Steven W. Smyrski	38312
George M. Sirilla	18221	Lynn E. Eccleston	35861	Jay M. Finkelstein	21082	Vivian S Shin	43919
Donald J. Bird	25323	Timothy J. Klima	34852	Michael R. Dzwonczyk	36787	Eric S. Chen	43542
Peter W. Gowdey	25872	David A. Jakopin	32995	W. Patrick Bengtsson	32456	Charanjit Brahma	46547
Dale S. Lazar	28872	Mark G Paulson	30793	Jack S. Barufka	37087		

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(include Zip Code)	97007		

(2) **INVENTOR'S SIGNATURE:** **Date:**

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(include Zip Code)	97219		

FOR ADDITIONAL INVENTORS, "X" box ☐ and proceed on the attached page to list each additional inventor.

☐ See additional foreign priorities on attached page (incorporated herein by reference).

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